

Design and Simulation of VCO for RF Transceivers with Low Power, Low Phase Noise and Wider Tuning Range using Silterra 130nm CMOS Technology

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Abstract

The performance of low-power transceivers is required to meet stringent specifications for an advanced wireless radio frequency (RF) application. The design topology in this paper is simulated to meet the specifications and operation of VCO for low power, low phase noise and wide tuning range in complementary metal oxide semiconductor (CMOS) 130nm technology for RF transceivers. The relationship between the phase noise, power consumption and frequency turning range is fully analyzed to further improve the performance of the voltage-controlled oscillator (VCO). The architecture of the VCO employs two sets of symmetrical cross couple split NMOS and PMOS with biased current sources operating in the triode region, and a resonator tank that achieves the desired low phase noise performance of about -110 dB/Hz at a tuning range of 4.1 to 4.5 GHz with a supply of 0.9 V. The control of the DC bias point reduces the conduction angle, which improves the current efficiency, power consumption and phase noise. The topology generates sufficient $-gm$ for the oscillator incorporation to mitigate the start-up issue of the VCO. At the center frequency of 4.38 GHz, the VCO serves as a promising solution for improving low power and low phase for wireless communication systems and RF transceivers applications. The design consumes very low power of 0.138 mW, achieves a phase noise of -110.53 dBc/Hz at 1 MHz offset, and a figure of merit (FoM) of -191.90 dBc/Hz.

Keywords: RF Transceivers, CMOS Technology, Oscillator, Resonator Tank, Tuning Range.



Introduction

Frequency generation is critical in modern wireless communication systems because it allows the desired radio signals to be extracted from an increasingly crowded spectrum. Through the advancement of new technologies, the integrated transceivers for wireless communication that have a small area with optimum performance improvement, are inexpensive, and low power have attracted a lot of researchers' attentions. The main component of a wireless system is the transceiver, in which the primary role is to send and receive data. Macaitis and Navickas (2015).

The phase locked loop (PLL) is primarily used as a frequency synthesizer in transceivers. Macaitis and Navickas (2017). A phase-locked loop (PLL) is a signal-controlled device which produces the same phase at the output as compared with an input signal. The Voltage Controlled Oscillator (VCO) is commonly used to produce the PLL's high frequency signal. The output frequency of a VCO oscillator is regulated either by voltage or current. Singh and Gurjar (2017), said that the output frequency oscillations can be regulated by varying the amplitude of the input voltage signal. LC-VCOs are widely used in wireless transceivers because of their excellent phase noise efficiency. Hai *et al.*, (2013). However, the application demand is for a design that is simple to implement, has a small chip area, and has low phase noise. Ring VCOs work with digital CMOS and take up little space on the chip.

The Ring oscillator (Ring-VCO) and the LC oscillator are the two most common forms of VCO (LCVCO). Ring-VCOs take up less space on the chip and have a wider frequency range, with worse phase noise efficiency than LC-VCOs. Although LC-VCOs work at higher frequencies, the tuning frequency range of their operation is limited and the inductors that are built into a chip take up a lot of space. Macaitis and Navickas (2015). LC-VCOs have a smaller tuning range than Ring-VCOs, but they perform better in terms of phase noise. Yu *et al.*, (2014).

The small variation in VCO gain is ideal for good phase noise, due to a limited frequency locking range, which becomes undesirable for wireless communications. In oscillators, phase noise is an unwanted conduct in the carrier frequency band manifested as noise. The carrier frequency band contains phase noise, which has a negative effect on the adjacent channel. Phase noise in VCO is caused by three major sources: MOSFETs, resistance in the tank, and the source of the tail current. Singh and Gurjar (2017).

A large varactor can be used in oscillators with continuous frequency tuning to achieve a broad range. A voltage-dependent capacitor is referred to as a MOS varactor with a measured capacitance that is proportional to the control voltage. Singh and Gurjar (2017). The losses of such a varactor, on the other hand, lower the resonator's quality factor and increase phase noise. Furthermore, for system applications, the output power is indeed a concern. While adding buffers or power amplifiers can increase output power, the cost increases the power consumption and size of the chip. Li *et al.*, (2013).

In today's world, there is a significant reduction in power levels, a large frequency range, and massive convergence. As a result, it is critical to design a low-power VCO with the lowest power and compare the phase noise efficiency to the latest state-of-the-art recordings to reduce the entire transceiver system's low-power usage to reduce battery capacity, restrictions, and energy drawn for a longer cell battery life span.

Problem Statement

The current exponential growth in wireless communication has surpassed the demand for more available channels in mobile communication application. This has imposed stringent requirements on the performance of the VCO especially on its phase noise in which it degrades as the number of channels and frequency increases. The phase noise

improvisation depends on the Q factor enhancement and it is an uphill task to ensure a high Q linear operation linearly with wide bandwidth. Besides, battery-powered devices are in high development, and it is crucial for a system to drain low power for longevity and sustainability, especially to suit into IoT/IoE Transceiver solution. In addition, achieving a wide tuning range while maintaining better phase noise performance seems to be a bottleneck in the current trend of VCO oscillators. RF researches face several limitations in improvising the sensitivity of oscillators towards achieving higher gain, better startup and persistently maintaining optimum current efficiency via conduction angle enhancement.

Objectives

The objectives of this paper are to design and simulate a voltage-controlled oscillator (VCO) for RF transceiver with extremely low power, low phase noise and wider tuning range using Silterra 130nm CMOS technology.

Literature Review

The design architecture by Gargouri *et al.*, (2011), achieved a ring voltage-controlled oscillator with two cross coupled load PMOS transistors. The method preserves the maximum frequency of the VCO unaffected, which leads to improvement of power consumption and phase noise of the voltage-controlled oscillators.

The delayed cell presented by Xuemei *et al.*, (2013), It is made up of a differential pair of Mn1 and Mn2 in the presence of a crossly-coupled load (i.e. Mp1 and Mp5), as well as two PMOS transistors that control the tuning range by changing the current of the output node. The delay cell's operation can be defined by changing the control voltage (Vctrl) on the gate of Mp3 & Mp6, which changes the charge up current of the delay cell's output load. Consequently, the delay time and frequency of the entire VCO can be controlled.

Parvizi *et al.*, (2008), designed architecture by using a delay cell with a two-stage ring VCO with a resistor between the outputs and inputs nodes to speed up the transfer rate at the output. The oscillating frequency is increased because of the main inverter and cross coupled transistors having the same transconductance. In other words, the two-stage ring VCO consumes less power to produce the same oscillating frequency.

Nejadhasan *et al.*, (2020), designed low phase noise and power consumption voltage-controlled oscillator with dual shaping currents, which are suitable for Internet of things (IoT) applications. The dual current shaping technique is used to improve the control ability of phase noise and power consumption. Low power VCOs are designed to improve FOM and reduce phase noise with dual current shaping technique. With the help of this, the main current of the circuit can be more controllable. The power dissipation and phase noise are decreased. The current shaping technique is used in the PMOS and NMOS biasing circuit structures to increase the frequency tuning range (FTR) without using a capacitor bank. Lai *et al.*, (2017).

Yan *et al.*, (2019), designed architecture for a frequency enhanced two-stage ring VCO with a larger tuning range by adding a resistor between the input and output of a delay cell, the

transmission gain is increased, and the oscillating frequency is produced with less power. A rail-to-rail efficient voltage tuning range is achieved by adjusting the tail current and the strength of the crossly coupled latches.

Sankararaju and Dharmar (2016), achieved a High Tuning, Low power CMOS Ring Voltage controlled Oscillator on 0.13m 1P8M CMOS technology for the differential and single-ended topology. The differential oscillator employs advanced technique and a modern composite load with inductive impedance to minimize delay per stage while also expanding the tuning range. The performance frequency tuning of the differential ring topology varies from 0.5 GHz to 9.5 GHz. This achieved power of 9mW, and measured phase noise of -85.3dBc/Hz at 1 MHz offset from the 5GHz carrier frequency. The inductive composite load oscillates between 6.3 and 13.9 GHz in a single end ring topology, carries 5.1 mW of power, and has phase noise of -81.5dBc/Hz at 1 MHz offset from the 10.1GHz of the centre.

There is a need to lessen the power issue, improve the phase noise and best output tuning range under the 5G NR frequency of the VCO, because of the VCO's widespread usage and consideration as a power-hungry block. This has placed strict demands on the VCO's output, particularly in terms of phase noise and power consumption, which worsens as the number of channels and the frequency of broadcast increase.

Material and Methods

The basics of VCO are explored followed by many design architectures in appreciating their priorities and process design flow. The design architecture is planned and simulated to keep all difficult trade-offs intact until the desired specification is reached. The simulation work on cadence virtuoso the PDK in Silterra CMOS 180nm technology and the performance parameters.

Table 1 shows the target specification of the proposed VCO design architecture, in which the simulation design analysis and flow chart need to meet the targeted specifications before achieving the proposed design objectives.

Table 1: Target specification of the VCO design

VCO Performance	
Performance	CMOS VCO
Silterra Technology [nm]	130
Voltage Supply [V]	< 1.2
Operating frequency [GHz]	< 4.6
Frequency range [GHz]	4.114 – 4.559
Power consumption [mW]	0.138
Power [dBm]	1.53
Phase Noise [dBc/Hz @1 MHz]	-110.529
Figure of Merit [dBc/Hz]	-191.9

VCO Design Topology

Table 2 shows the table of components parameters sizes of the VCO design.

Table 2: System Components List, instances and their values.

S/N	NAME	INSTANCES	VALUES
1	NMOS Transistors	N1 and N2	FW = 8, F = 4, Total width = 32
2	PMOS Transistors	P1 and P2	FW = 8, F = 8, Total width = 64
3	Varactor capacitor	Cvar	FW = 500 nM, FL = 130 nM, Finger in X = 19, Finger in Y = 19. Multiplier = 1
4	Vtune Range	VTUNE	0 --- 1.8V
4	Capacitors	C1, C2, C3	1p
5	Inductor	LO	1.32 nH
6	Voltage source	VDD	900 mV
7	Ground	GND	0V

The VCO is a frequency-controlled oscillator with voltage or current controlled at the output frequency. Ring, relaxation, and LC oscillators are the three types of oscillators that are commonly used. The first two realizations are simple and easy to manipulate, but these oscillators have low phase noise. That is why they are rarely used in RF applications. Because of their excellent phase noise efficiency, LC VCOs are commonly used in RF applications. Kim *et al.*, (2008).

A single transistor can be used to build an LC circuit. In VCO, the LC tank's topologies are the most significant. The main goal of topology selection is to achieve perfect oscillation while minimizing losses. The Inductor (Q_{L1}) and capacitor (Q_{C1}) quality factors are expressed as.

$$Q_{L1} = \frac{R_1}{\omega L_1} \dots\dots\dots(1)$$

$$Q_{C1} = \omega C_1 R_1 \dots\dots\dots(2)$$

The inductor's quality is considered in this design since the capacitor's quality factor is much higher than the inductors.

LC Topology

LC oscillator topologies are divided into three categories:

Cross-coupled NMOS is the cross connection between the two MOS at lower side of figure 1 (i.e. N_1 & N_2) in parallel with the inductor, Vdd and ground with a cross coupled NMOS feedback configuration with negative resistance detected at the drains and it is expressed as:

$$R_{neg} = -\frac{2}{g_m} \dots\dots\dots(3)$$

Cross-coupled PMOS is the same cross connection between the upper side of figure 1 (i.e P₁ & P₂) in parallel with inductor and Vdd and ground. The negative resistance used to achieve continuous oscillation *R_{neg}* must be less than or equal to the LC tank's parallel resistance arrangement. Setting either V_{GS} or V_{DS} to VDD determines the NMOS topology's DC bias (Kral *et al.*,1998).

The drain current in the saturation area is expressed as:

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \left(\frac{w}{l} \right) (V_{GS} - V_{TH})^2 \dots\dots\dots(4)$$

Also, the Trans conductance, *G_m* as

$$G_m = \frac{\partial I_{DS}}{\partial V_{GS}} \left(\frac{w}{l} \right) (V_{GS} - V_{TH}) \mu_n C_{ox} \dots\dots\dots(5)$$

Cross coupled complementary MOS is the cross-couple combination of both PMOS and NMOS with the same current flow in the topology, but the size of the PMOS transconductance is twice large as that of NMOS. Because the electron flow in NMOS is faster, the need to double the size of PMOS arises to accommodate the same flow of electrons. The negative resistance of the CMOS pair is given as;

$$R_{negative} = -\frac{2}{G_{mn} + G_{mp}} \dots\dots\dots(6)$$

The key difference between both topologies is that the disparity voltage swing caused by current flow is limited by the CMOS type meanwhile raises noise sources due to the increased number of active transistors but has less power dissipation. Hou *et al.*, (2010).

To reduce power consumption, the CMOS cross-coupled topology is used. Since the similar current flows via the PMOS and NMOS crossed couple pairs, the PMOS topology's available transconductance can be double that of the NMOS topologies with the same bias. Therefore, the key benefit of the cross-coupled CMOS configuration is that the PMOS cross-couple pairs increase negative transconductance, lowering the current drawn. As a result, the circuit's power is reduced while maintaining the same voltage supply. The topology is required to be optimized with bias currents to achieve the optimum operating point of the VCO.

VCO Design Schematic Topology

The capacitor in the LC VCO Circuit Topology is replaced by fine-tuned varactors. Figure 1 shows a typical LC VCO varactor topology used. *V_{tune}* is the tuning voltage to be swept from 0V – 1.8V. Since the varactors are PN junctions, they must be reverse biased, changing the capacitance value. Since the inductors act as a short circuit to Vdd in DC, the inductance

is halved, with the varactor capacitance generating a sine voltage. Therefore, the AC + DC voltage is present at nodes VP and VN. The VCO control voltage can be varied from ground to Vdd to keep the varactors reverse biased.

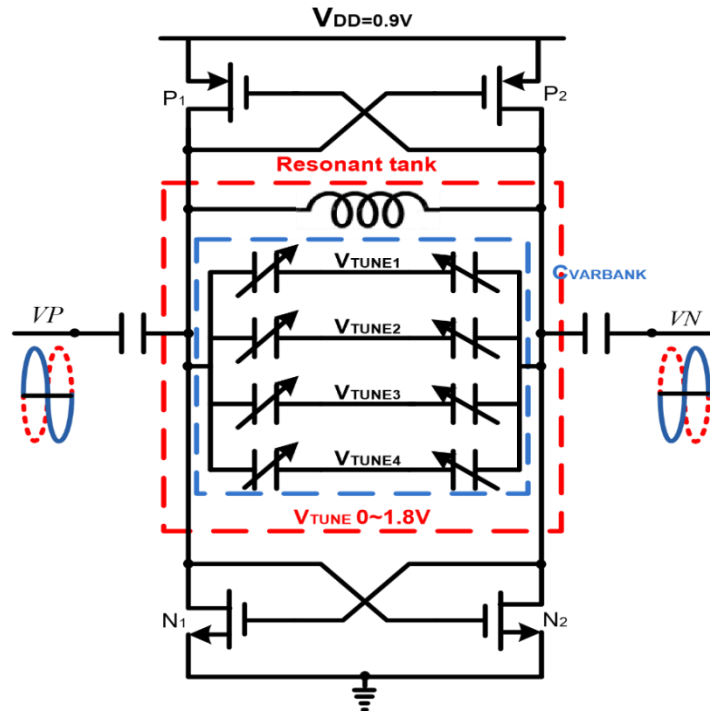


Figure 1: Schematic of LC VCO Topology with Varactors.
Figure 2 depicts the concept flow chart for the VCO design.

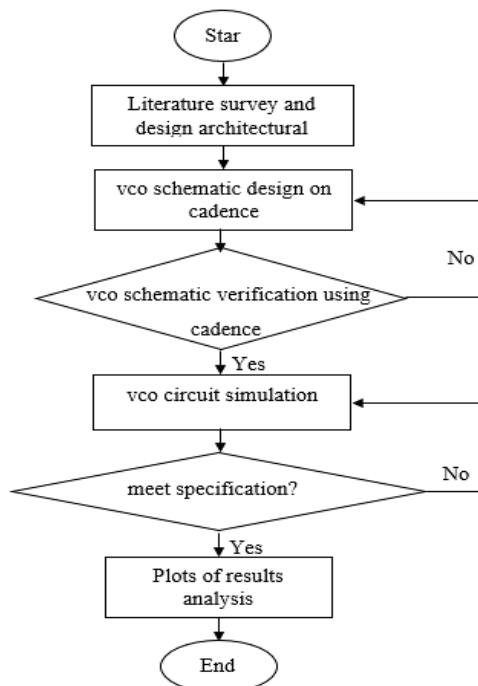


Figure 2: Flow Chart of VCO Design Process

Simulation Results and Discussion

The following analysis; d.c, harmonic balance (hb) and harmonic balance noise (hbnoise) are selected, added, and enabled in the ADE L window and configured for the run of the respective analysis with Vtune of the varactor configuration set up. After analysis selection, the netlist and run icon were clicked to execute the simulation. When finished, the plotted waveform will be checked and executed by clicking on the result, direct plot, to be plotted. A new window on ADE L will pop up to plot the simulation results for the analysis mentioned above with transient stability as in figure 3.

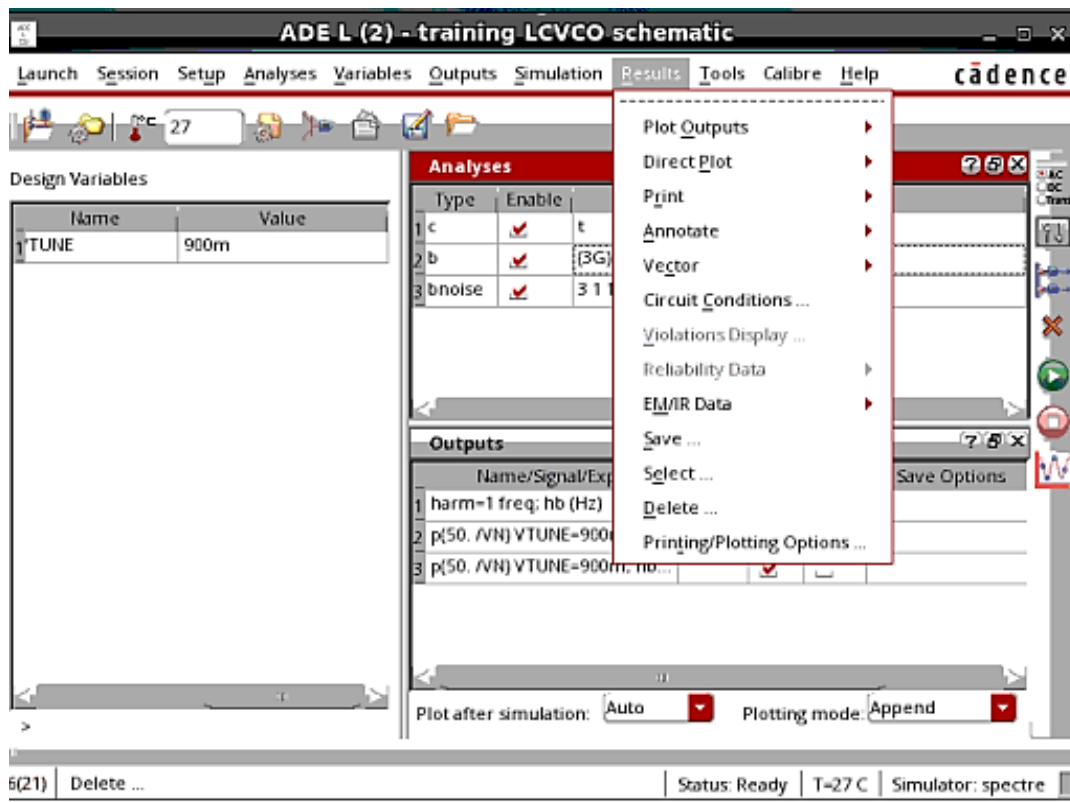


Figure 3: The Plot of Simulation Results Window

After the configuration setup for the analysis mentioned, the design achieved the plotted results for better phase noise, low power consumption and wider tuning range as shown in figures 4, 5 and 6 respectively.

Simulated Phase Noise Result

The phase-noise of the design is achieved by improving the quality factor of the inductor. The LC tank circuit inductor's series resistance should be reduced to a minimum to determine when the oscillator encounters phase noise criteria. A nonlinear harmonic balance simulation is used. At 1MHz offset tuning frequency, the phase-noise of the oscillator has a minimum and maximum value of -110.506 dBc/Hz and -112.497 dBc/Hz, respectively, within the tuning voltage range of 0 to 1.8 V as in figure 4.

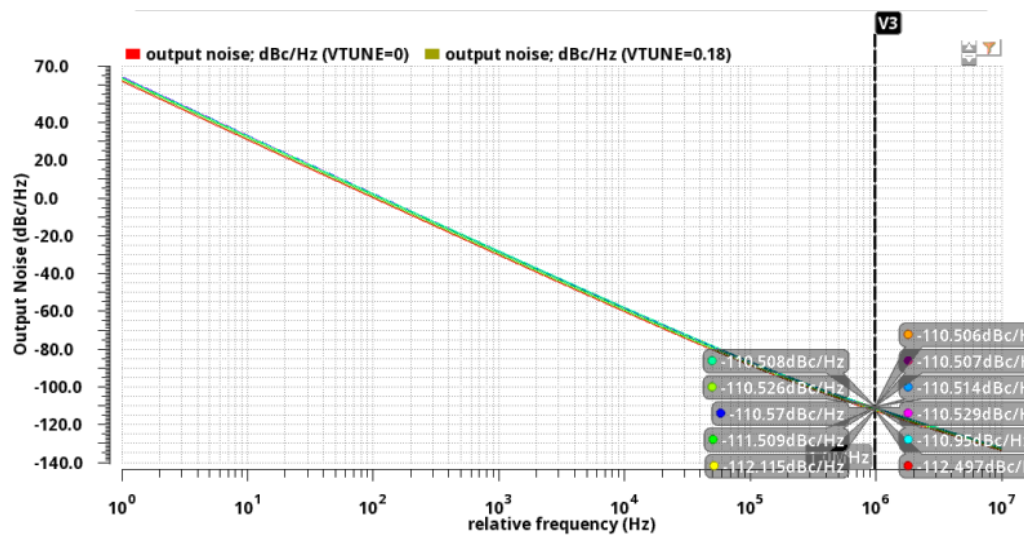


Figure 4: The Results of the VCO Harmonic Balance Noise Response Simulation

Simulated Output Power Result

The output power of the oscillator is the maximum power it can deliver based on circuit specifications. The output power ranges over the tuning frequency spectrum, which is also defined at 4.5GHz, the output power of this design is 1.54dBm (0.138 mW) as in the figure 5.

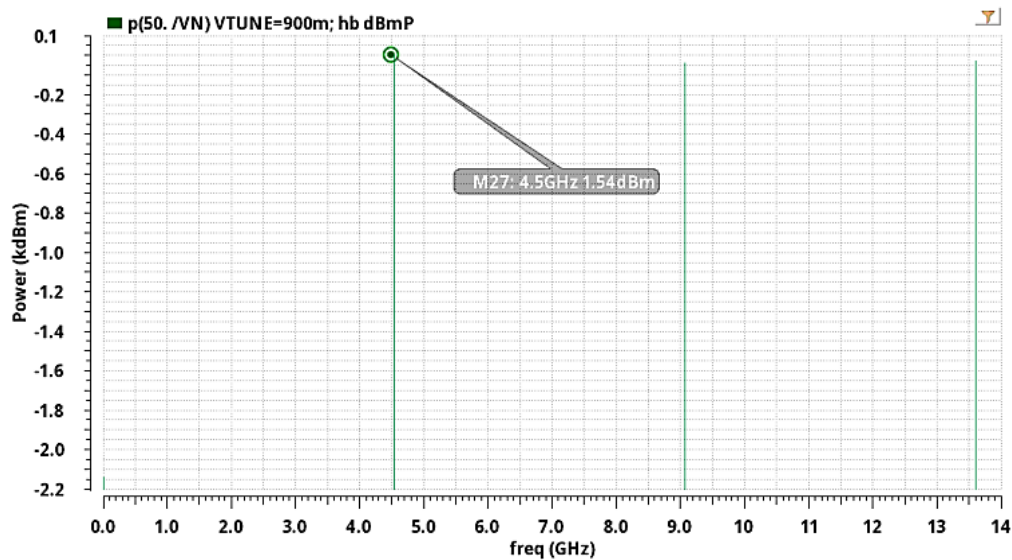


Figure 5: The Result of Output Power Analysis

Simulated Frequency Tuning Range (FTR) against Tuning Voltage Result

The Cadence Virtuoso Spectre Cell view window simulator was used to measure the plotted VCO tuning range for 5G NR frequency. The tuning voltage (Vtune) is swept from 0V to 1.8 V. The control voltage and oscillation frequency of VCOs designed for frequency synthesis in phase locked loop (PLL) applications require a linear relationship, resulting in a range of

min and max boundaries. The simulated frequency versus tuning voltage is shown in Figure 6.

Figure 6 illustrates the simulated VCO frequency tuning range against tuning voltage. It was discovered that the frequency varies from 4.114GHz to 4.559GHz, within the control voltage ranging from 0V to 1.8V After simulations.

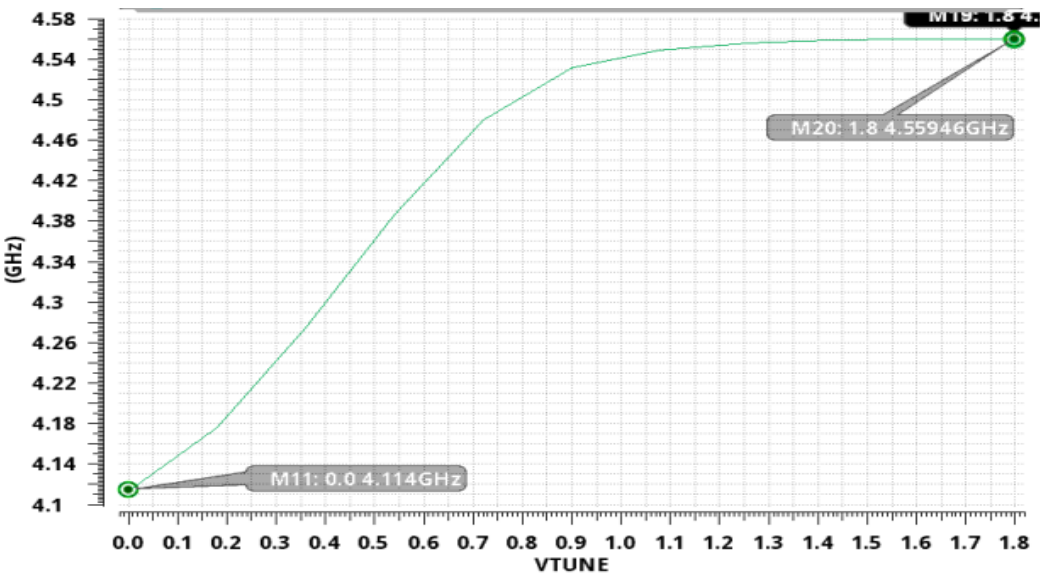


Figure 6: The Result of frequency tuning range against tuning voltage.

Table 3 shows the output performance summary of each important parameter for the proposed design architecture.

Table 3: Performance Summary Results of the VCO Design

parameters	Tech [nm]	Vdd [V]	F _{osc} [GHz]	Tuning Range [GHz]	Phase [dBc/Hz] @ 1MHz offset	Noise	Power [mW]	FoM [dBc/Hz]
Results	130	0.9	4.38	4.114 – 4.559	-110.529		0.138	-191.9

Conclusions and Recommendations

The proposed VCO design architecture was concluded with the reduction of VCO power consumption to a very low of about 0.138 mW, lower phase noise of -110.529 dBc/Hz at 1MHz offset and a wider tuning range from 4.11 to 4.56 GHz for 5G NR frequency bandwidth was achieved. The proposed VCO circuit architecture was developed using Silterra CMOS 130nm technology and simulation was carried out using the virtuoso analog design environment (ADEL) simulation window in Cadence Spectra RF simulator to analyse the design for high performance results of the LC tank, resulting in achieving more favourable performance of the design and power reduction, which is an essential part of every modern communication system and RF transceiver application.

The recommendations are;

- The VCO design frequency turning range can be further reduced by adjusting the varactor finger length.
- The design can further be configured by integrating different VCO architectures into the PLL to enhance the flicker noise up conversion investigation and optimization of phase noise with low power consumption.
- The design can be further improved by employing at different classes architecture and incorporated inside the PLL to enhance the investigation on the flicker noise upconversion.

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